Customer No.: 31561
Application No.: 10/709,125
Docket NO.: 11808-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A NAND flash memory cell row, comprising:

a substrate;

a plurality of gate structures, disposed over the substrate, each of the gate structures comprising a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer and a control gate;

a plurality of doped regions, disposed in the substrate between the gate structures, wherein the gate structures are connected in series;

a plurality of erase gates, disposed over the doped regions and between the gate structures;

a plurality of spacers, disposed between the gate structures and the erase gates;

a plurality of dielectric layers, disposed between the erase gates and the doped regions;

a first select gate and a second select gate, disposed on each of the sidewalls of two outermost gate structures respectively;

a plurality of select gate dielectric layers, disposed between the first select gate and the substrate and between the second select gate and the substrate;

a drain region, disposed in the substrate, wherein the drain region is

disposed on one side of the first select gate corresponding to the gate structures,; and

a source region, disposed in the substrate, wherein the source region is disposed on one side of the second select gate corresponding to the gate structures.

2. (original) The NAND flash memory cell row of claim 1, wherein the erase gate fills up spaces between the gate structures.

3. (original) The NAND flash memory cell row of claim 1, wherein a thickness of the select gate dielectric layer is about 90 Å to 100 Å.

4. (original) The NAND flash memory cell row of claim 1, wherein the inter-gate dielectric layer comprises silicon oxide/silicon nitride/silicon oxide composite layer.

5. (original) The NAND flash memory cell row of claim 1, wherein the floating gate comprises polysilicon layer doped with arsenic.

6. (original) The NAND flash memory cell row of claim 1, wherein a thickness of the dielectric layer is about 300 Å to 500 Å.

7. (original) A NAND flash memory cell array, comprising:

a plurality of memory cell rows, disposed two-dimensionally and arranged in a memory cell array, wherein each of the memory cell rows comprises:

a substrate;

a plurality of gate structures, disposed over the substrate, wherein each of the gate structures comprises a tunneling dielectric layer, a floating gate, an inter-gate dielectric layer, and a control gate disposed on the substrate successively;

a plurality of doped regions, disposed between the gate structures in the substrate, wherein the gate structures are connected in series;

a plurality of erase gates, disposed over the doped regions and between the gate structures;

a plurality of spacers, disposed between the gate structures and the erase gates;

a plurality of dielectric layers, disposed between the erase gates and the doped regions;

a first select gate and a second select gate, disposed on each of the sidewalls of the two outermost gate structures respectively;

a plurality of select gate dielectric layers, disposed between the first select gate and the substrate, and the second select gate and the substrate;

a drain region, disposed in the substrate, wherein the drain region is on one side of the first select gate corresponding to the gate structures; and

a source region, disposed in the substrate, wherein the source region is on one side of the second select gate corresponding to the gate structures ;

a plurality of word lines, arranged in parallel along column direction, and each of the word lines is coupled to the control gates of the gate structures in a column;

a plurality of bit lines, arranged in parallel along row direction, each of the bit lines is coupled to the drain region of the first select gate in a row;

a source line, coupled to the source regions of the second select gates in

the same column respectively; and

a plurality of erase gate lines, arranged in parallel along column direction, and coupled to the erase gates in the same column.

8. (original) The NAND flash memory cell array of claim 7, wherein the erase gate fills up spaces between the gate structures.

9. (original) The NAND flash memory cell array of claim 7, wherein a thickness of the select gate dielectric layer is about 90 Å to 100 Å.

10. (original) The NAND flash memory cell array of claim 7, wherein the inter-gate dielectric layer comprises silicon oxide/silicon nitride/silicon oxide composite layer.

11. (original) The NAND flash memory cell array of claim 7, wherein the floating gate comprises polysilicon layer doped with arsenic.

12. (original) The NAND flash memory cell array of claim 7, wherein a thickness of the dielectric layer is about 300 Å to 500 Å.

Claims 13-29 (canceled)